

FIG. 1

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Rx_DV = 0												
Rx_Cyc												
Tx_Cyc												
Word 0	11	10	9	8	7	6	5	4	3	2	1	0
Word 1	00	01	01	00	01	01	00	01	01	00	01	00
Word 2	Even	SQL	RST-RQST	PM-mode	00	00	Even	CRS	Duplex	Seed	1_Er	Rx_Er

FIG. 2



11	10	9	8	7	6	5	4	3	2	1	0	
				Rdata0	Rdata1	Rdata2	Rdata3	Rdata4	CRS	Rdata5	Rdata6	Rdata7

FIG. 3



11	10	9	8	7	6	5	4	3	2	1	0	
				Rdata0	Rdata1	Rdata2	Rdata3	Rdata4	CRS	Rdata5	Rdata6	Rdata7

Mdout

Rx\_Cyc = 1

Rx\_Dv = 1

FIG. 4



FIG. 5



11	10	9	8	7	6	5	4	3	2	1	0
Mdstart	Mdin	TX_EN = 1	Tdata0	Tdata1	Tdata2	Tdata3	Tdata4	Tdata5	Tdata6	Tdata7	
SEL = 0		TX_EN = 0	rsrvd	rsrvd							

Command\_Word

FIG. 6



Mdin		IDLE	ST	OP	Reg Addr (10 bits)	Data (16 bits)
000...0		1		01		
Mdout						IDLE

FIG. 7



FIG. 8. Sequence of bus states for a write operation. The sequence starts with an IDLE state, followed by a bus idle period, then a bus cycle period, and ends with an IDLE state.

Mdin	IDLE	ST	OP	Reg Addr (10 bits)	Wait Time	IDLE	000...0	Data (16 bits)
	000...0	1	10		0001		000...0	
Mdout				IDLE	0001			

FIG. 8

01 - 0001  
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U.S. DEPARTMENT OF COMMERCE

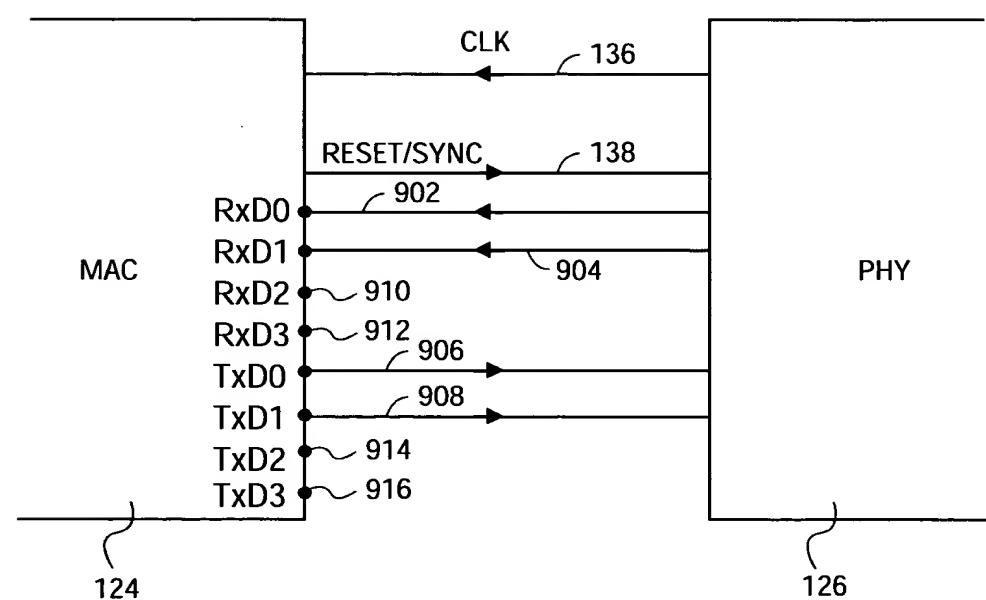


FIG. 9

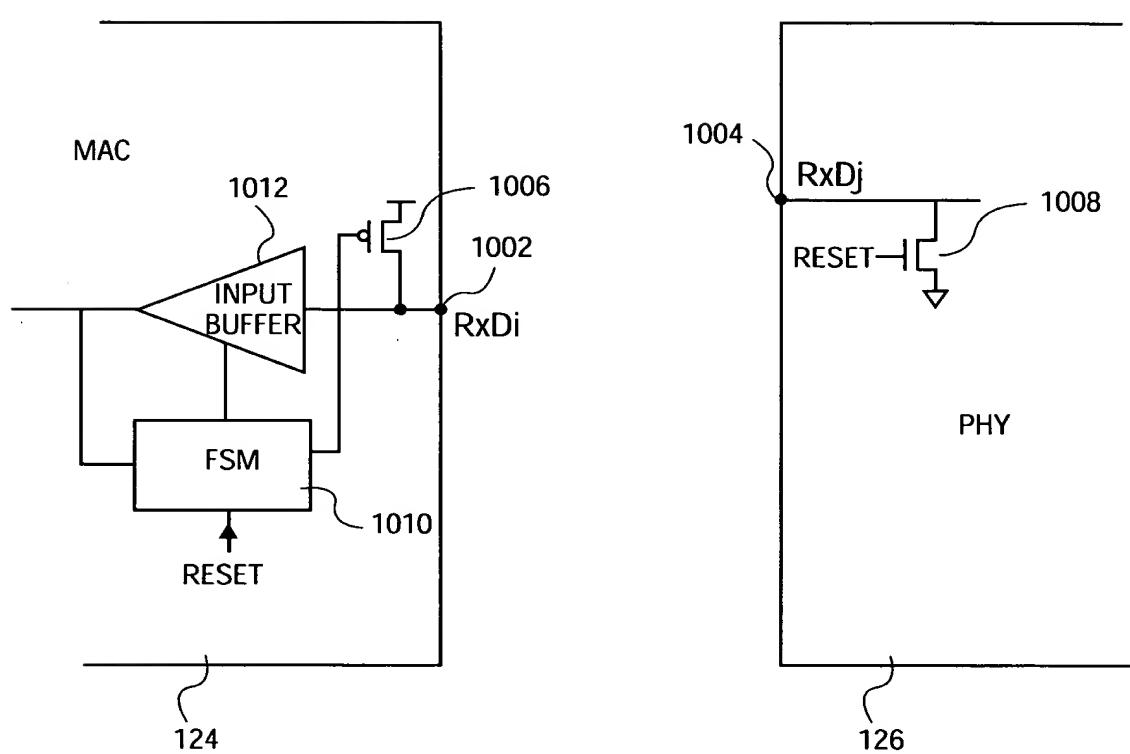


FIG. 10

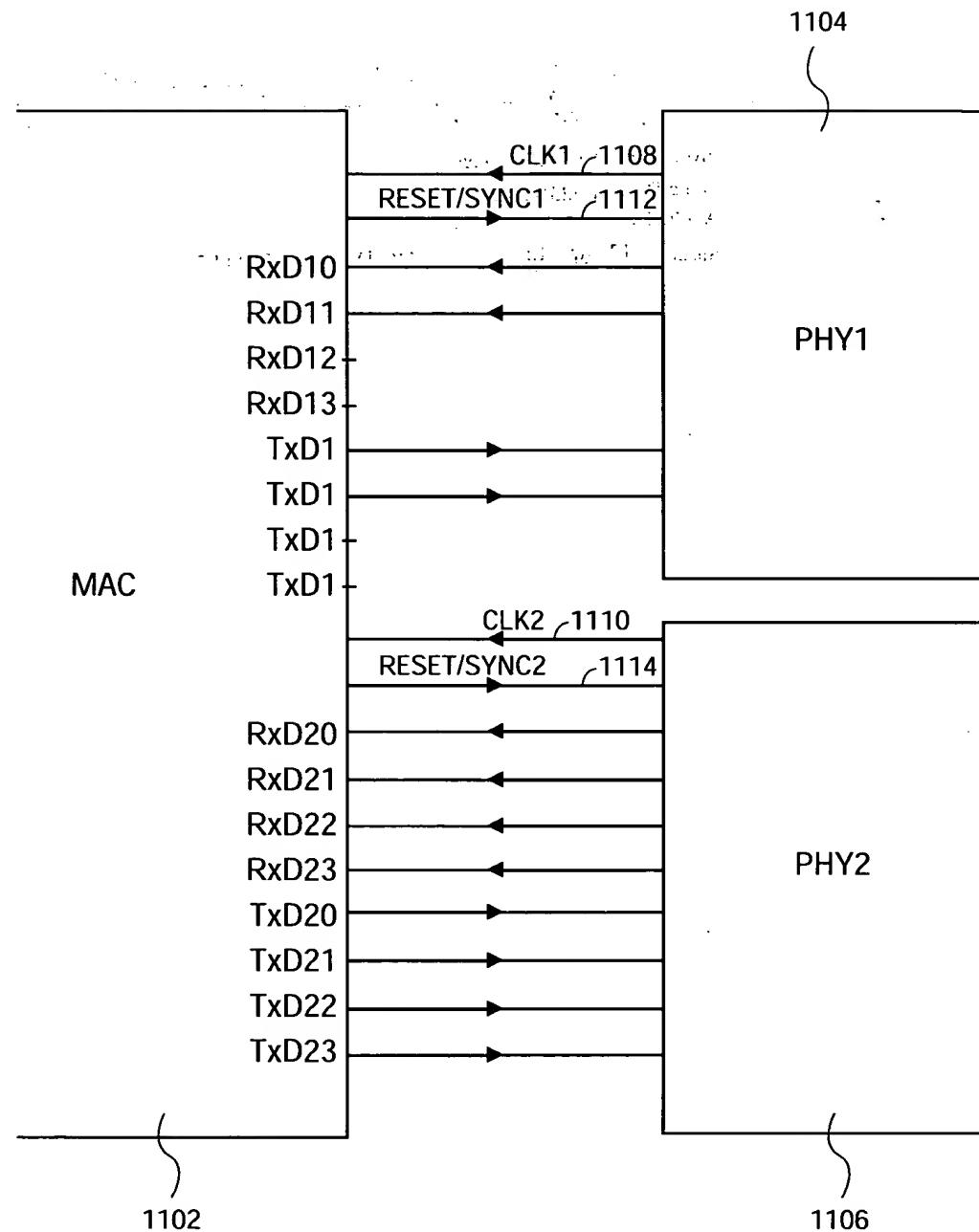


FIG. 11

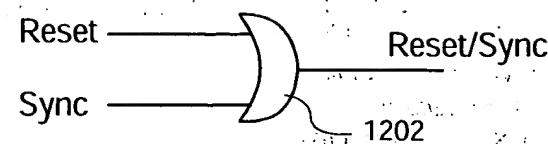


FIG. 12A

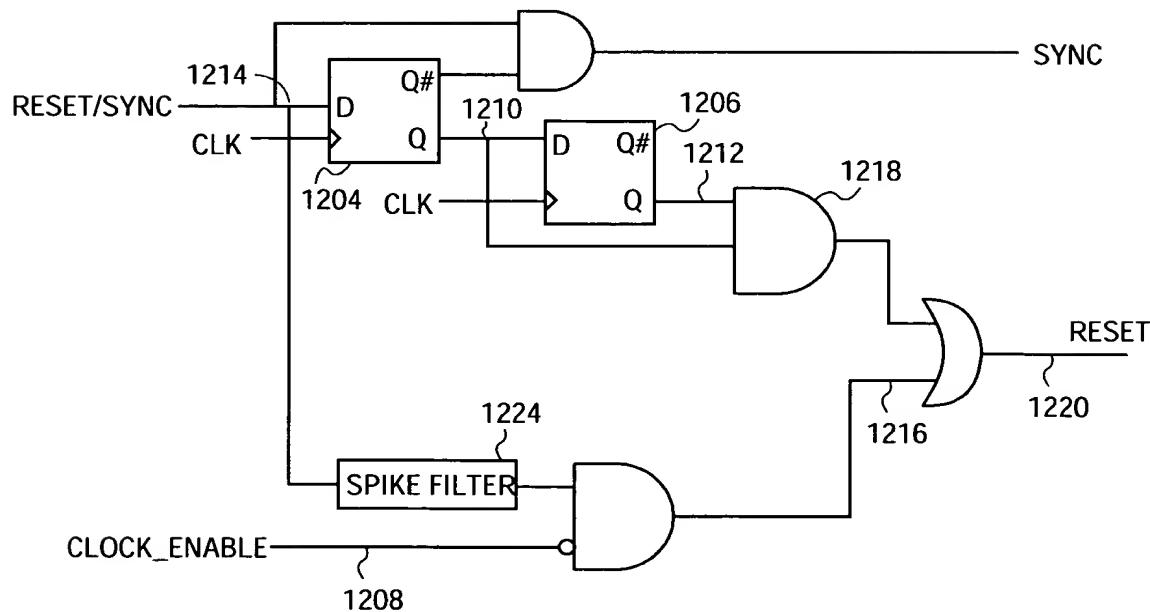


FIG. 12B